## Main Features

- **High Sensitivity Full-frame CCD Sensor**
- **2300 x 3500 Resolution with 10 µm Square Pixels**
- **100% Aperture Pixels**
- **12-bit Dynamic Range**
- **Very Low Noise: 65 dB SNR**
- **Binning and ROI Modes**
- **LVDS or CameraLink™ Data Format (Base Configuration)**
- **High Data Rate: 25 Mpixels/s**
- **Flexible and Easy to Operate via RS-232 Control**
  - **Trigger Mode: Free-run or External Trigger Modes**
  - **Binning 2 x 2 and 4 x 4, Up to 5 ROI**
  - **Exposure Time**
  - **Gain: -6 to 27 dB by Steps of 0.04 dB**
  - **Offset: 0 to 255 LSB**
  - **3-Shot Color Operation**
  - **Test Pattern Generation**
- **Single Power Supply: $24V_{DC}$**
- **High Reliability – CE and FCC Compliant**
- **F (Nikon) Mount Adapter (Lens not Supplied)**

## Description

This camera is designed to meet high performance and quality requirements while providing ease of use. Atmel manages the entire manufacturing process, from the sensor to the camera. The result is a camera that operates in 12 bits, with dedicated electronics that provide excellent signal-to-noise ratio. Due to the 100% aperture pixel, the sensitivity of the camera is fairly high, even in near infrared.The programmable settings let the user work with different integration times, gains and offsets. The external trigger allows the user to synchronize the camera on an external event while the 3-shot color mode allows very high resolution for color image acquisition.

## Applications

The performance and reliability of this camera make it well suited for the most demanding applications such as film and document scanning, semiconductor and PCB inspection, DNA analysis, metrology or X-ray imaging.

# Black and White 8 Megapixels LVDS and CameraLink™ Digital Cameras

## CAMELIA M1 LV 8M
## CAMELIA M1 CL 8M

5319C–IMAGE–02/04

## Improvements

The Camelia 8M has been redesigned to:

- Add new features, which include:
  - Gain: 941 steps from -6 to 27 dB
  - Offset: 0 to 255 LSB
  - Test pattern: ramps up from 0 to 2298 pixel values on each line
  - Median filter: to remove 1 x 1 and column defects
  - 12 or 8 bits output format selection
- Improve the electro-optical performances, in particular by:
  - Reducing power consumption from 8.5 to 5.5W, using a new front panel and internal heat sink. This lowers the CCD temperature by 5° C, thus decreasing the magnitude of “white pixels”.
  - Decreasing the typical temporal noise from 2.7 to 2.4 LSB
- Interface with more standard and more cost-effective cables
- Improve reliability

The Camelia M1 8M is CE and FCC compliant.

Main changes for the user include:

- New additional commands for gain, offset and test pattern
- Interface connectors:
  - DATA & SYNC are 3M MDR connectors with improved availability, the same pinout but different mechanics
  - The RS-232 is a D-Sub 9 female connector for full-duplex transmission
  - The power supply connector has a camera standard pinout
  - The TTL CONTROL is a new D-Sub 9 male connector avoiding the use of a Y cable
- A new rear panel (see position of connectors on Figures 1 and 2 on page 3.)

**Figure 1.** LVDS Imaging System

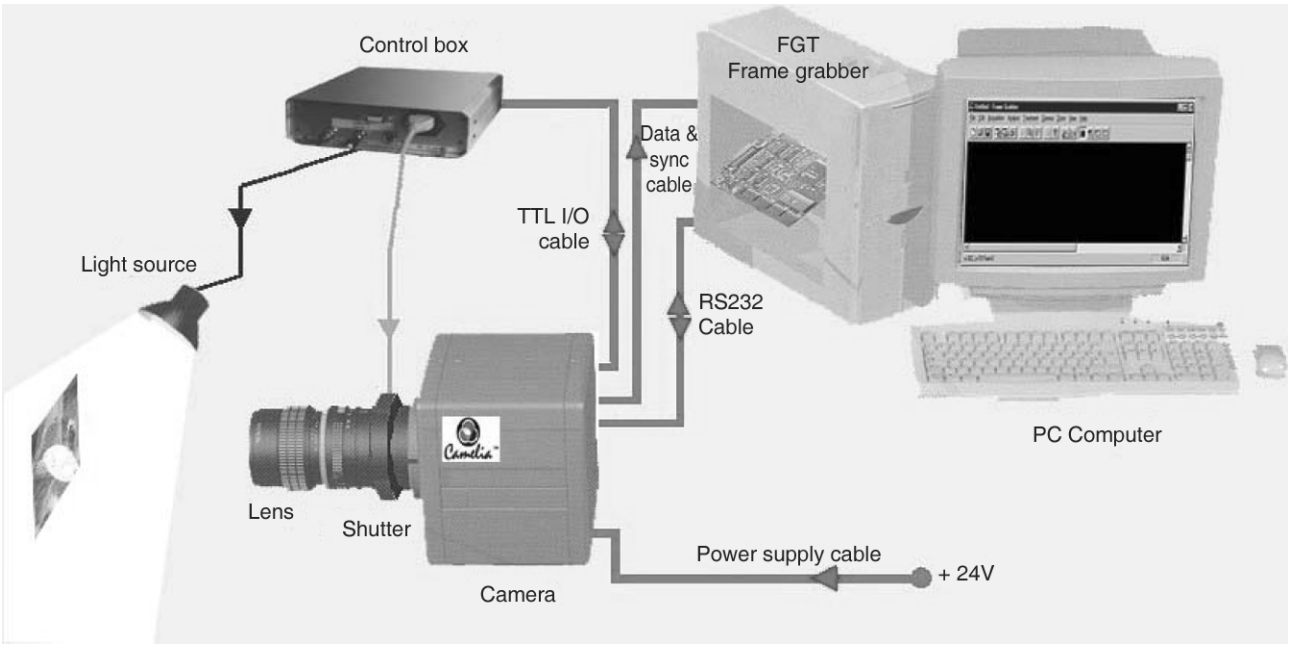
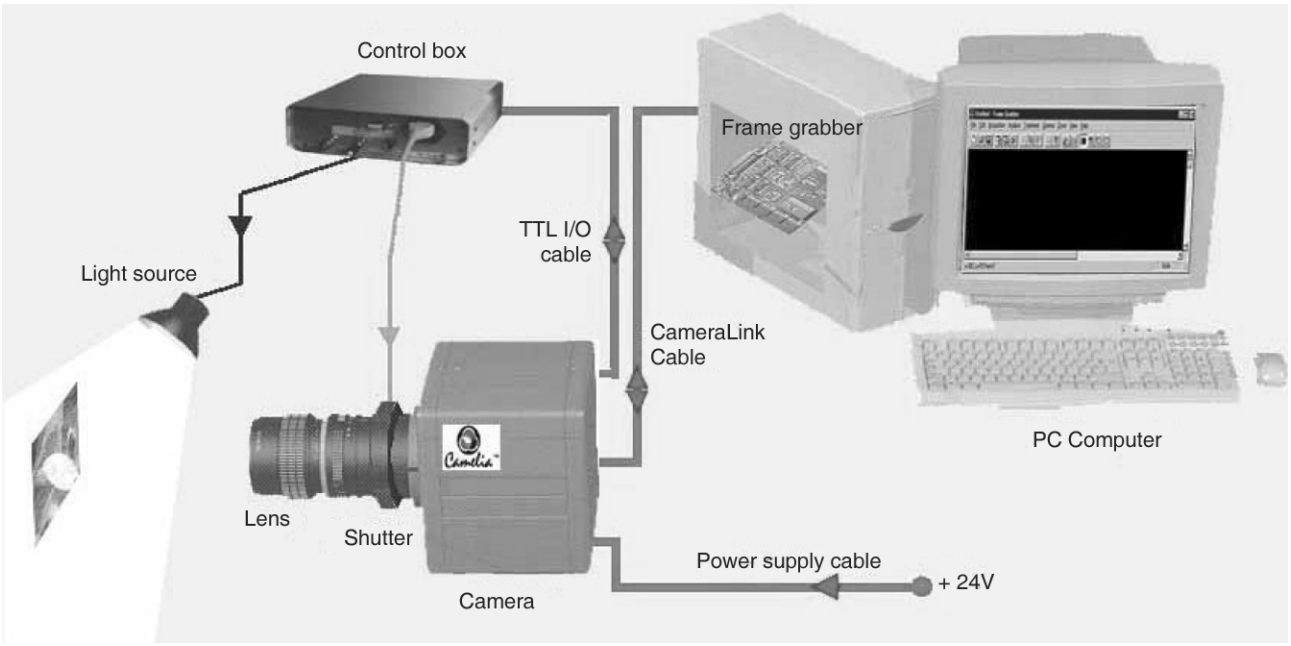



**Figure 2.** CameraLink Imaging System



The Camelia camera is powered by a single 24V power supply. It is configurable via the computer's serial port (by using either CommCam software or a standard RS-232 communicator such as TTY or Hyperterminal) for LSD cameras. The Camelia is also configurable via the serial communication of CameraLink™ for CameraLink cameras. It also sends digital video data.

As the Camelia's CCD is a full-frame sensor, the user must use either pulsed lighting or a chopper/shutter in front of the camera to obtain only incident lighting on the CCD during the integration time. The user must design an electro-optical interface to drive the camera, shutter/chopper or lighting by using the SHUTTER signal emitted by the camera. If required, the system can send an external trigger or external ITC (integration time control signal) to the camera.

The BG38 filter is essential to obtain correct white balance on color cameras and for use with standard optics (for achromaticity purposes).

The following elements are not provided by Atmel:

- Shutter (LCD or mechanical)
- BG38 (Anti-infrared) filter
- Control box
- Lens
- Light source
- +24V power supply
- Computer

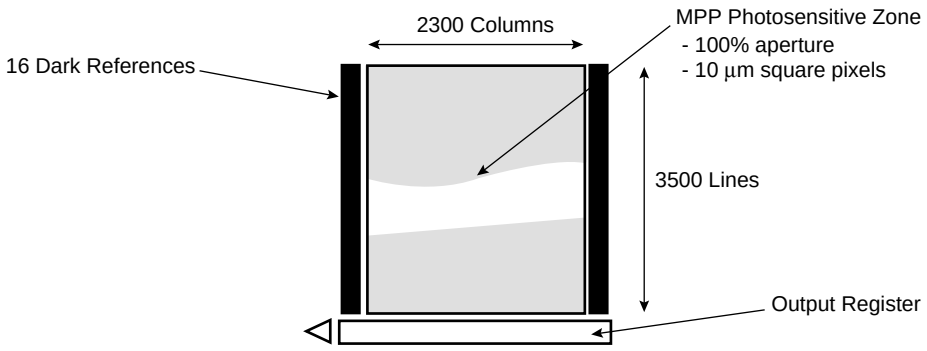
For a complete explanation on the utility of the BG38 filter and the shutter, please consult the associated FAQ and the sample images on Atmel's "Camera Documentation and Software" CD-Rom.

## CCD Description

### Image Format

35.0 mm (V) x 23.0 mm (H)

**Figure 3.** Sensor Organization




Note: The camera does not output to the 16 dark references.

### Active Pixels

**Table 1.** Active Pixels

| Mode (set via serial com) | Image Size (H x V) | Timing Diagram Correspondence |
|---|---|---|
| No binning | 2300 x 3500 | H = M<br>V = N |
| 2 x 2 pixel binning | 1150 x 1750 | |
| 4 x 4 pixel binning | 574 x 875 | |

### Readout Register

The readout register appears along the small side of the image area (vertical image).

### Pixel Geometry

Pixels are 10 µm x 10 µm with an aperture ratio of 100%.

### Over-illumination Capability

Over-illumination control can be activated or inhibited (see “Serial Communication” on page 12):

- OFF: control inhibited. This position is recommended if over-illumination control is not required for the application.
- ON: control activated.
- When binning is disabled, the control is typically efficient at up to eight times the saturation light at an exposure time = 100 ms..

## Camera Specifications

LSB (Least Significant Bit): 12 bits correspond to 4095 LSB.

### Absolute Maximum Ratings

| | |
|---|---|
| Storage temperature: | -20 to +70° C |
| Operating temperature: | 0 to +50° C |
| Operating humidity (non-condensing): | < 80% at +35° C |
| Vibration: | 2g sinusoidal, from 10 to 100 Hz |
| Power supply: | +20 to +28V |

### Weight

- Camera with F mount ring: 1400g
- Camera without F mount ring: 1200g

### Electro-optical Performance

Requirements:

- The camera should operate at an ambient temperature of 20° C.
- The camera should operate in binning 1 x 1 mode, nominal gain 0 dB (G = 173) and have no processing filter.

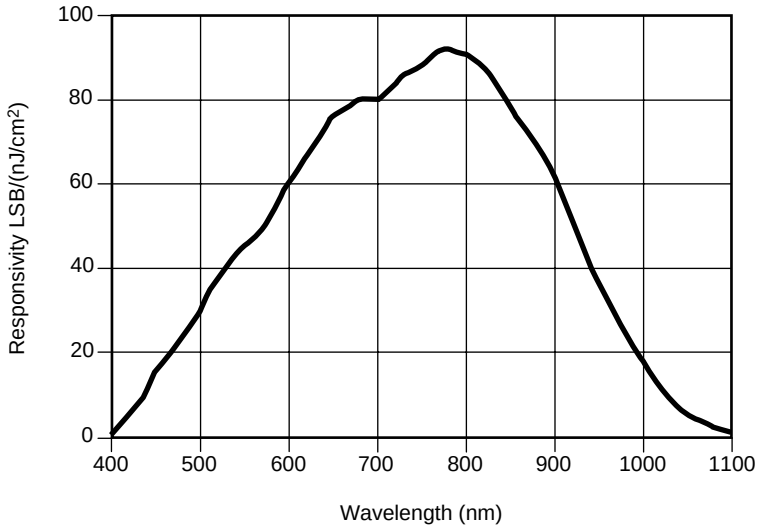
**Table 2.** Electro-optical Performance

| Parameter | Symbol | Typical Value | Unit |
|---|---|---|---|
| Full scale value(1) | VPE | 4095 | LSB |
| Temporal noise(2)(3) | VN | 2.4 | LSB |
| Dark signal non-uniformity(3)(4) | DSNU | 2 | LSB |
| Dynamic range(5) | DY | 1700<br>64.6 | <br>dB |
| Responsivity(6) | R | 51.43 | LSB/(nJ/cm$^2$) |
| Resolution(7)<br>Horizontal transfer function at Nyquist<br>Vertical contrast transfer function at Nyquist | <br>CTFh<br>CTFv | <br>20%<br>20% | <br>–<br>– |
| Over-illumination capability(8) | – | 8x | – |
| Electrons to LSB conversion | – | 15 | e-/LSB |
| Current consumption(9) | I | 230 | mA |

Notes:
1. Full-scale value VPE: maximum digital video signal
2. Temporal noise VN: rms value in darkness; measured by subtracting 2 images, pixel to pixel, at 40 ms of integration time
3. This parameter depends on the integration time and CCD temperature. Thermal noise doubles with every 16° C temperature increase. The dark signal doubles with every 8° C temperature increase. An internal clamp can correct the mean value of this phenomena.
4. Dark signal non-uniformity: rms value; excludes blemishes
5. Dynamic range DY = VPE/VN measured at 40 ms of integration time
6. Responsivity conditions: 3200K light source powered between 200 and 1100 nm, measured on the sensor
7. Resolution conditions: VIDEO = 2000 LSB and red light source used
8. Over-illumination control ON and integration time = 100 ms
9. Measured at 24V

## Spectral Responsivity

**Figure 4.** Spectral Responsivity




Note: nJ/cm$^2$ measured on the sensor

## Image Grade Specification

- Defect sizes
  - Blemish: 1 x 1 defect
  - Cluster: blemish grouping of not more than a given number of adjacent defects:
    1 x 1 < cluster 1 size ≤ 2 x 2
    2 x 2 < cluster 2 size ≤ 5 x 5
  - Column: one-pixel-wide column with more than 7 contiguous defective pixels
  - Defect separation: defects are separated by no less than D minimum pixels in any direction
- Defects in darkness
  - Blemish or cluster: pixel(s) whose signal deviate(s) more than 150 LSB
  - Column: column whose signal deviates more than 15 LSB
- Defects under illumination
  - Blemish or cluster: pixel(s) that deviate(s) by more than +20% or -30% from the *average* pixel
  - Column: column which deviates by more than 10% from the *average* column

### Defect Test Conditions

- Room temperature = 20° C
- Integration time in darkness = 100 ms
- Camera operating in binning 1 x 1 mode
- Light source: halogen 3200K with BG38 (2 mm thick) IR cut- off with f/11 aperture
- Test under illumination at 50% saturation level
- No software correction performed

## Classifications

**Table 3.** Image Grade Classifications

| Grade | Blemishes | | Cluster 1 | | Cluster 2 | | Column | |
|---|---|---|---|---|---|---|---|---|
| | Total | D min | Total | D min | Total | D min | Total | D min |
| E | ≤500 | 3 | ≤30 | 50 | ≤6 | 100 | ≤5 | 150 |
| H | ≤300 | 3 | ≤10 | 50 | 0 | – | 0 | – |

## CCD Window Specification

- Thickness = 1.2 mm ± 0.05
- Glass index at 588 nm: n = 1.5255
- Admitted defects rate: 0 inclusions > 10 µm
- Transmittance > 98% in the range of 400-700 nm
- Transmittance > 82% in the range of 700-1000 nm
- Flatness of the CCD window < 100 um (concave)
- Flatness of the CCD chip must be within 30 µm

## Camera Features

### Regions of Interest (ROI )

**Caution**: This function has been available since October 2001 starting with the camera S/N: 01321093. For older cameras, these commands are not available and can corrupt the EEPROM (see “Camera Identification” on page 14).

The Camelia 8M can operate in multi ROI mode, allowing masking of different regions of the image and thus increasing the frame rate by a reduced readout time.

The user can define up to five masked windows. In addition, the starting and ending addresses for each window can be specified.

The time reduction is approximately 92 µs per masked line.

Follow these two steps (under serial communication):

- Enter the list of starting and ending addresses with the command: Y=ssss/eeee/ssss/eeee/…/eeee/
- Enter the number of regions masked with the command: F=X (X=0 to 5)

**Rules**

The line addresses must be multiples of 4 (to be compliant with the binning).

The image starts at Line 0 and ends at Line 3499 and the smallest area consists of 4 lines.

The commands must be sent in the following order: “Y=…” then “F=…”.

For FGT software users, the number of lines in the FGT settings must be resized.

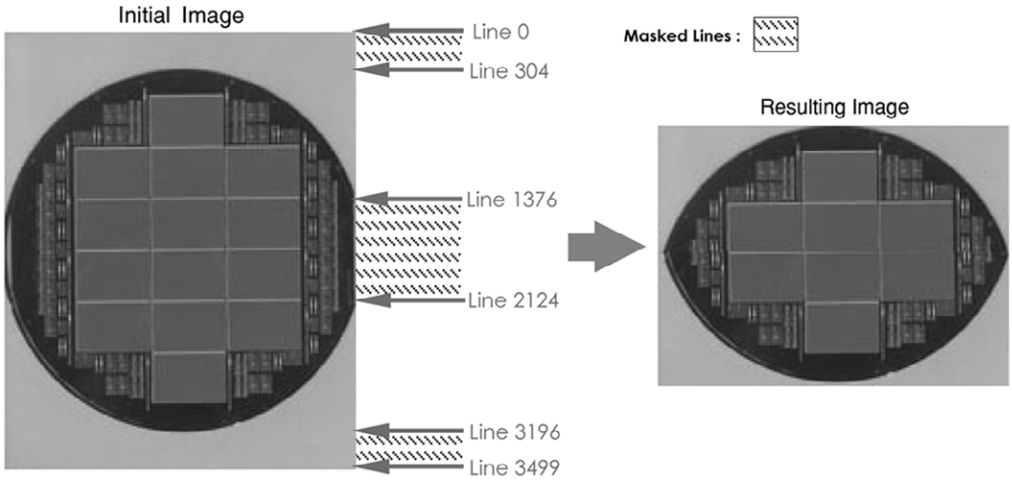
**Example**

Three regions masked in the wafer image defined below:

- The first 304 lines at the top of the image (blue background)
- 748 lines in the center of the image (two center lines of the wafer)
- The last 304 lines of the image (blue background):
  - "Y=0/304/1376/2124/3196/3499/"
  - "F=3"

In this example, the readout time will be reduced by 1356 line, which are equivalent to 125 ms.

**Figure 5.** Readout Time



## Gain and Offset

The video gain and offset signal processing can be adjusted by setting the gain and offset via the serial communication:

- Gain adjusted from -6.1 to 27 dB: G = code 0 to 941
- Nominal gain (factory configuration) is 0 dB: G = code 173
- Offset adjusted from 0 to 255 LSB: O = code 0 to 255
- Gain is applied to the video signal before the addition of offset

## Over-illumination Control

Over-illumination control can be activated or inhibited (set via the serial communication):

- A = 0 - OFF: this position is recommended if over-illumination control is not required for the application.
- A = 1- ON: control is activated and is effective at up to 8 times the sensor's saturation level.

It is important to know that this feature is optimum at an exposure time of 100 ms. Its efficiency is decreased when the exposure time is reduced.

## Test Pattern

In normal mode, the digital video signal from the CCD sensor is available at the LVDS output interface.

For test purposes a fixed digital pattern is generated and can be made available instead of the video signal at the LVDS output interface.

The digital pattern is ramped up from 0 to 2298 LSB code (line width); each line presents the same pattern:

This is useful in validating the connection to the acquisition system before adjustment operations relative to the image capture.

Selection is set by the Test Pattern Generation command:

- CCD sensor : M = 0
- Test Pattern : M = 1

## Median Filter

A median filter can be applied to sensor signals to remove 1 x 1 defect pixels or 1 pixel width columns thus avoiding subsequent software processing. This filter produces a smoothing effect on the image.

- Median filter OFF: M = 0
- Median filter ON: M = 2

## Pixel Output Format

Digital output pixels can be set to 8 or 12 bits:

- 12-bit width: M = 0, 1 or 2
- 8-bit width (8 MSB): M = 3

## 3-Shot Color Operation

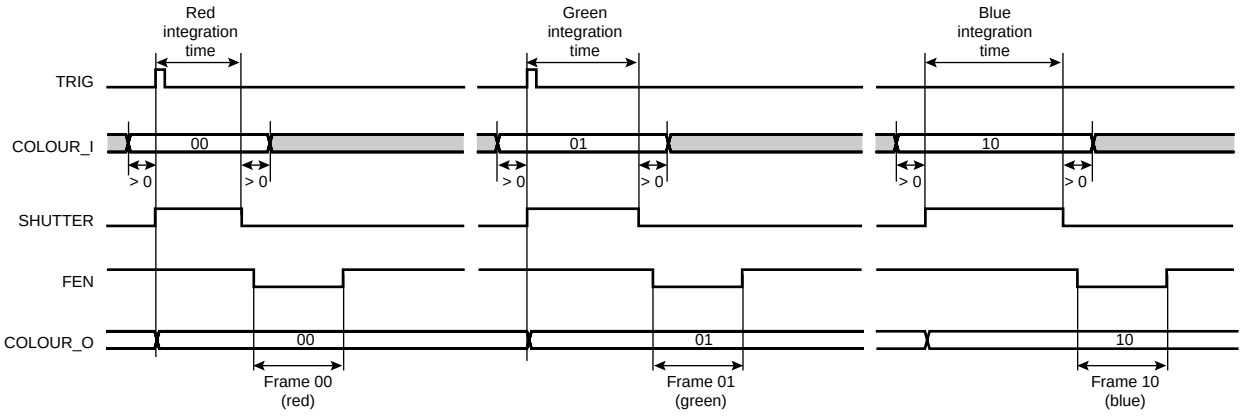
In 3-shot color mode, each image is made up of 3 frames: red, green, blue and 1 optional additional frame (infrared for example):

- The camera must operate either in external trigger mode or in Integration Time Control (ITC) mode.
- For each image, the user selects the color of the next frame by setting COLOUR_I1 and COLOUR_I2 input signals. COLOUR_I1, _I2 must be valid during both the TRIG signal's rising edge (or the ITC signal's falling edge) and the SHUTTER signal's falling edge (see Figure 6).
- The color definition is the following:

| COLOUR_I2 | COLOUR_I1 | Frame Color |
|---|---|---|
| 0 | 0 | Red |
| 0 | 1 | Green |
| 1 | 0 | Blue |
| 1 | 1 | User defined i.e. Infra Red |

- The integration time can be adjusted differently for each color (set viathe serial communication). This provides enhanced signal-to-noise ratio for the color with the lowest sensitivity (i.e the blue).
- Each frame requires a TRIG_ITC signal.
- The Camelia 8M camera synchronizes COLOUR_I1, _I2 with the rest of the timing and sends COLOUR_O1, _O2 to:
  - The FGT frame grabber for LVDS cameras
  - The CameraLink frame grabber as the 2 most significant bits of data PDATA(13,12)

**Figure 6.** Color Timing Diagram



# Serial Communication

## Serial Configuration

The camera configuration is set by an RS-232 or CameraLink serial interface.

The RS-232 configuration is:

- Full duplex/without handshaking (the camera is configured in DCE/Modem)
- 9600 baud, 8-bit data, no parity bit, 1 stop bit

The CameraLink serial interface configuration is:

- 9600 baud, 8-bit data, no parity bit, 1 stop bit

## Serial Commands

The following features are available:

**Table 4.** Serial Commands

| Function | Serial Configuration | Comment | Serial Command |
|---|---|---|---|
| Timing mode | 3 modes:<br>- continuous (free running)<br>- external trigger<br>- external ITC | | <br>T=0<br>T=1<br>T=2 |
| Binning | 3 modes:<br>- no binning<br>- 2 x 2 pixel binning<br>- 4 x 4 pixel binning | <br>Image size: 2300 (H) x 3500 (V)<br>Image size: 1150 (H) x 1750 (V)<br>Image size: 574 (H) x 875 (V) | <br>B=0<br>B=1<br>B=2 |
| Gain | Range from:<br>- G = -6.1 dB<br>- G = 27 dB | Steps of around 35 mdB (gain curve is linear) | <br>G=0<br>G=941 |
| Offset | Range from:<br>- 0 LSB<br>- 255 LSB | Steps of 1 LSB | <br>O=0<br>O=255 |
| Shutter | 3 modes:<br>- inactive (always open)<br>- active<br>- inactive (always closed) | | <br>S=0<br>S=1<br>S=2 |
| Shutter delay | 4 positions:<br>- 1 ms<br>- 10 ms<br>- 20 ms<br>- 40 ms | | <br>D=0<br>D=1<br>D=2<br>D=3 |
| Over-illumination control | 2 modes:<br>- inactive<br>- active | | <br>A=0<br>A=1 |
| Black and white or 3-shot color mode | 2 modes:<br>- black and white<br>- 3-shot color | | <br>C=0<br>C=1 |

**Table 4.** Serial Commands (Continued)

| Function | Serial Configuration | Comment | Serial Command |
|---|---|---|---|
| Black and white integration time or 4th color integration time | Value: 1 to 2000<br>Unit: ms<br>Active modes: monochrome and 3-shot color | Must be an integer<br>Ex: 120 for 120 ms<br>120.4 not allowed | Ex:<br>I=120 |
| Red integration time | Value: 1 to 2000<br>Unit: ms<br>Active mode: 3-shot color | Must be an integer<br>Ex: 120 for 120 ms | Ex:<br>J=120 |
| Green integration time | Value: 1 to 2000<br>Unit: ms<br>Active mode: 3-shot color | Must be an integer<br>Ex: 120 for 120 ms | Ex:<br>K=120 |
| Blue integration time | Value: 1 to 2000<br>Unit: ms<br>Active mode: 3-shot color | Must be an integer<br>Ex: 120 for 120 ms | Ex:<br>L=120 |
| ROI: Number of windows | 0 to 5 windows | | Ex:<br>F=2 |
| ROI: Windows addresses | Line start/Line Stop … | Must be an integer divisible by 4<br>Line Stop >3<br>First Line = 0; Last Line = 3499 | Ex:<br>Y=1824/2252/<br>3156/3499/ |
| Test pattern generation medial filter processing | M=0: Sensor image<br>M=1: Pattern image<br>M=2: Sensor image filtered<br>M=3: 8 bits format | <br>To check power, transmission...<br>To remove 1 x 1 pixel defects<br>8 Most Significant Bits | M=0<br>M=1<br>M=2<br>M=3 |
| Special commands | | Camera identification readout<br>User camera identification readout<br>Software version readout<br>Camera configuration readout<br>Current camera configuration record<br>Default camera configuration restoration | !=0<br>!=1<br>!=2<br>!=3<br>!=4<br>!=5 |
| User camera ID | $= String of Char | Writing and record of the user camera identification | $= |

Note: ROI commands have been available since October 2001 starting with the camera S/N: 01321093. For older cameras, these commands are not available and can corrupt the EEPROM. If in doubt, please contact our hotline before using the ROI function (See “Camera Identification” on page 14).

## Command Syntax

- The valid syntax is: S=n(CR) where:
  - S: command identification (S is a single character in upper case)
  - n: setting value
  - (CR): means "carriage return" (ASCII code = 13)
  - No spaces or tabs may be inserted between S, =, n and (CR)
  - For the Camelia 8M only, each address value is followed by “/”: Y=ssss/eeee/….eeee/
- Example of a valid command: I=500(CR) (sets the integration time to 500 ms)
- Examples of non-valid commands:
  - I=500(CR): no space
  - i=500(CR): i instead of I
  - I=3000(CR): 3000 is out-of-range
  - Y=ssss/eeee/ssssseeee/: a “/” is missing

## Settings Validation

New settings are clocked and become valid at the end of the readout phase. This means that new settings written before the end of the readout of image N will be used for image N+1. New settings written after the readout of image N and before the end of the readout of image N+1 will be used for image N+2.

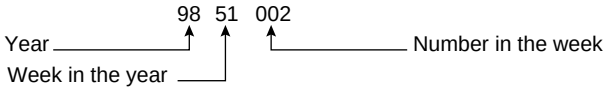
## Camera Identification

A character string stored in the EEPROM contains the product model, its version and its serial number.

It is read by sending: !=0(CR)

The serial number is detailed as follows:

**Figure 7.** Serial Number




## Customer Identification

The customer identification is a string of characters (25 characters maximum).

- It is set and stored in the EEPROM by sending $=xx..xx
- It is read by sending !=1(CR)
- The camera identification has an evolutive format. For application-specific needs, you should use the customer identification.

## Reading Firmware Version

When the camera receives !=2(CR) it returns the firmware version.

## Reading Current Settings

When the camera receives !=3(CR) it returns its current settings.

## Storing the Current Configuration

When the camera receives !=4(CR) it stores the current configuration in the EEPROM.

### Factory Configuration

When the camera receives !=5(CR), it returns its factory settings:

A=0(CR)
C=0(CR)
G=173(CR)
O=16(CR)
S=1(CR)
B=0(CR)
T=0(CR)
I=0100(CR)
J=0100(CR)
K=0100(CR)
L=0100(CR)
D=2(CR)
M=0(CR)
F=0(CR)
Y=(CR)(not set)
>OK(CR)

## Error Codes

| Description of Return Values | |
|---|---|
| >1 | Out-of-range failure |
| >2 | Syntax error failure |
| >3 | Message too long failure |
| >4 | Internal failure |
| >5 | Undefined function failure |
| >6 | Internal failure |
| >7 | Internal failure |
| >8 | Internal failure |
| >9 | Internal failure |
| >10 | FPGA configuration failure |

## Timing

2 x 2 and 4 x 4 pixel binning can be used to enable previewing modes. The preview mode is only available in black and white, otherwise the user has to use the overlay mode (correction and software LUT are not applicable on displayed images).

**Table 5.** Timing Mode

| Mode | Frame Readout Time | Line Readout Time | Max Frame Rate |
|---|---|---|---|
| No binning B=0 | 370 ms | 104 µs | 2.67 f/s |
| 2 x 2 pixel binning B=1 | 200 ms | 114 µs | 4.91 f/s |
| 4 x 4 pixel binning B=2 | 110 ms | 134 µs | 8.82 f/s |

## LVDS Camera Timing

Three timing modes are available: continuous, external triggered and Integration Time Control (ITC).

The signals in Figures 8 to 11 starting on page 17 are described in Table 6:

**Table 6.** LVDS Frame Timing

| Signal | Name | Description | Cam. In/Out | DATA & SYNC Pins | TTL CONTROL Pins |
|---|---|---|---|---|---|
| LEN | Line ENable | Low state active when pixel is part of line | Out | 26/27 | – |
| FEN | Frame Enable | Low state active when lines are part of frame | Out | 3/4 | – |
| SHUTTER | Shutter sync | External shutter Trig output signal (high level active) | Out | 21/22(1) | 1(1) |
| TRIG | Trigger | External Trigger input signal (rising edge) | In | 46/47(1) | 2(1) |
| ITC | Integration Time Control | External ITC input signal (falling/rising edges) | In | 46/47(1) | 2(1) |
| PCK | Pixel Clock | Internal master data clock signal at 25 MHz | Out | 1/2 | – |

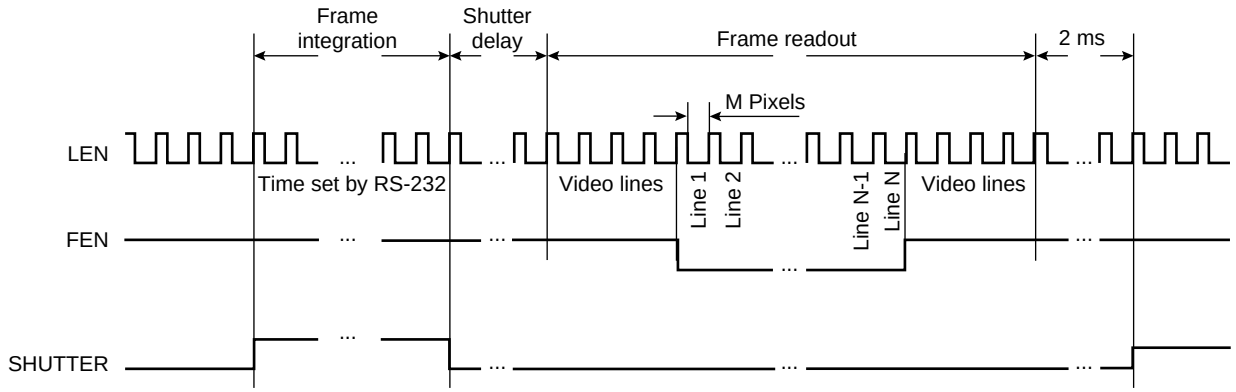
Notes:
1. Signal present on both connectors
2. Pixel is defined as valid (part of the frame) when both LEN and FEN signals are at a low level.
3. The maximum latency (called Td) after of 1 readout line time defined below depends on the binning mode. In binning 1 x 1 mode, this delay is around 104 µs.
4. Minimum time at high level of the LEN signal is 10 µs (transfer time between two lines).
5. Minimum time at high level of the FEN signal is 4 lines readout time (around 416 µs).
6. Shutter delay is adjustable via Commcam or RS-232 commands (1, 5, 10 or 20 ms).

**Continuous: T=0**

The camera delivers frames continuously:

- Frame N+1 integration starts as soon as the readout for frame N has been completed.
- The integration time is set by RS-232.
- The video lines (before and after the valid frame) are 4 + 4 for binning 1 x 1 (and also 1 + 1 for binning 4 x 4).

**Figure 8.** LVDS Continuous Timing Diagram

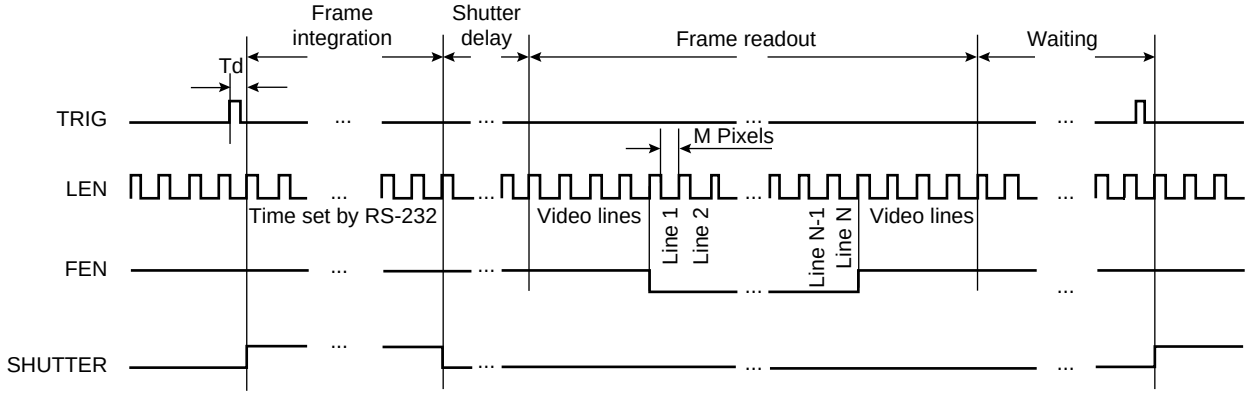



**Operation with External Trigger: T=1**

The start of integration is controlled by the user by the external signal TRIG:

- TRIG's rising edge activates the start of frame integration. This rising edge is synchronized by the camera with a latency of Td (time delay equivalent to a readout time for a line: see notes in Table 6 on page 16).
- The integration time is set by RS-232.
- The TRIG signal period must be greater than the sum of the integration time and frame readout time.
- The video lines (before and after the valid frame) are 4 + 4 for binning 1 x 1 (and also 1 + 1 for binning 4 x 4).

**Figure 9.** LVDS External Trigger Timing Diagram

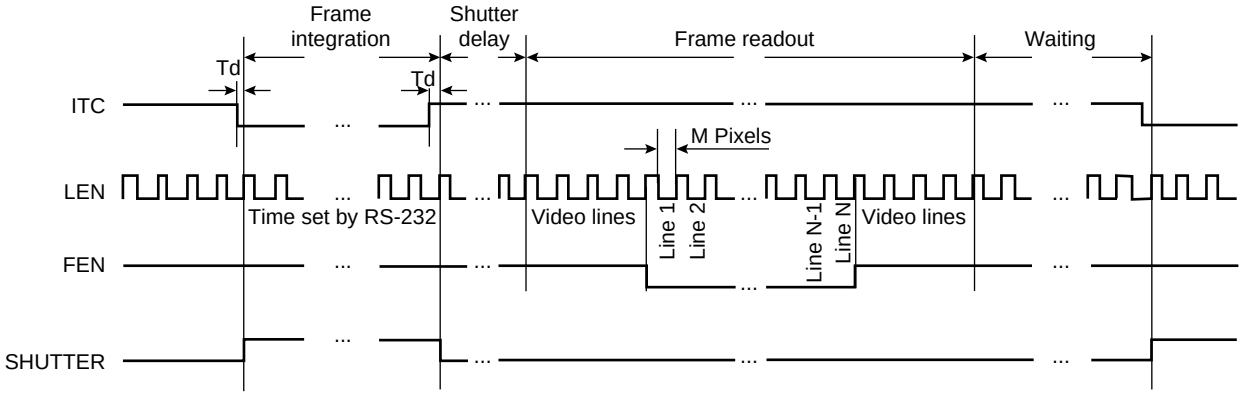


**Operation with Integration Time Control: T=2**

The integration is fully controlled by the user by the external signal ITC:

- ITC's falling edge activates the start of frame integration. This falling edge is synchronized by the camera with a latency of Td (time delay equivalent to a readout time for a line: see notes in Table 6 on page 16).
- ITC's rising edge activates the stop of frame integration. This rising edge is synchronized by the camera with the same latency as Td.
- The ITC signal period must be greater than the sum of the integration time (defined by ITC low) and frame readout time.
- The video lines (before and after the valid frame) are 4 + 4 for binning 1 x 1 (and also 1 + 1 for binning 4 x 4).

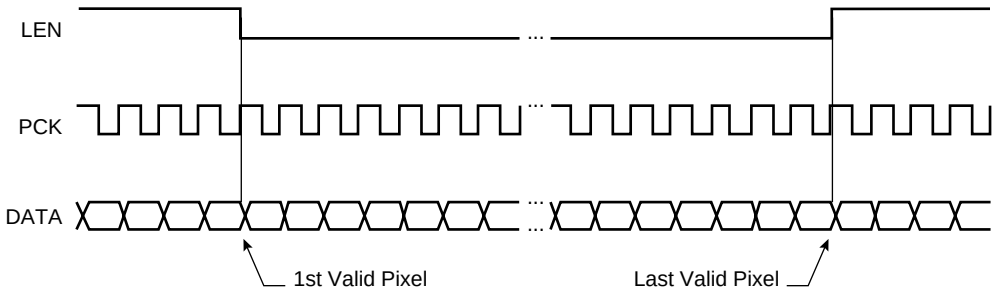
**Figure 10.** LVDS Integration Time Control Timing Diagram




**Line Timing**

- The duty cycle of the PCK is 50%
- The rising and falling edges are 1.5 ns
- The pixel clock PCK and data rate are 25 MHz in binning mode 1 x 1, 12.5 MHz in binning mode 2 x 2 and 6.25 MHz in binning mode 4 x 4
- The minimum setup time of Data, LEN and FEN, to the rising edge of PCK is 10 ns.
- The minimum hold time of Data, LEN and FEN, after the rising edge of PCK is 10 ns.

**Figure 11.** LVDS Line Timing Diagram



## CameraLink Camera Timing

Three timing modes are available: continuous, external triggered and Integration Time Control (ITC).

The signals in Figures 12 to 16 starting on page 19 are described in Table 7:

**Table 7.** CameraLink Frame Timing

| Signal | Name | Description | Cam. In/Out | Camera Link Connector | TTL CONTROL Connector |
|---|---|---|---|---|---|
| LVAL | Line Valid | High state active when pixel is part of line | Out | yes | no |
| FVAL | Frame Valid | High state active when lines are part of frame | Out | yes | no |
| SHUTTER | Shutter sync | External shutter Trig output Sig. (high level active) | Out | no | Pin 1(1) |
| TRIG | Trigger | External Trigger Input Signal (rising edge) | In | CC1+/ CC1-(1) | Pin 2(1) |
| ITC | Integration Time Control | External ITC Input Signal (falling/rising edges) | In | CC1+/ CC1-(1) | Pin 2(1) |
| PCK | Pixel Clock | Internal Master Data Clock Signal at 25 MHz | Out | yes | no |

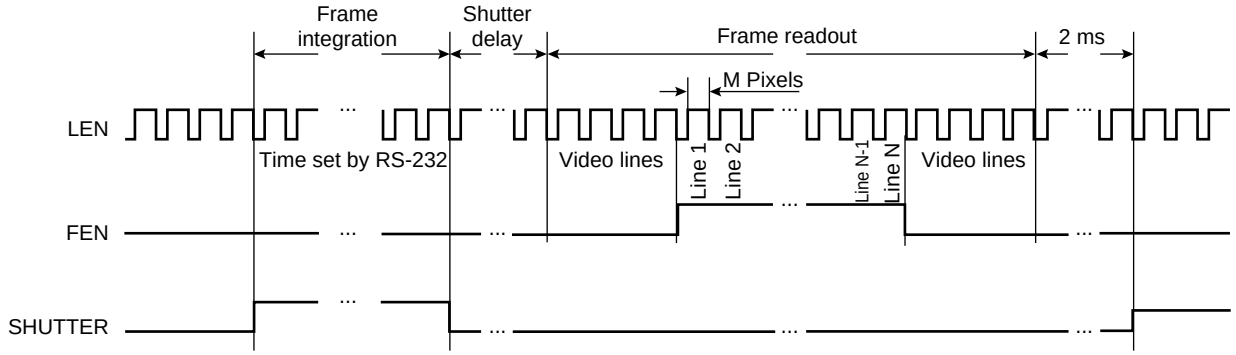
Notes:
1. Signal present on both connectors
2. Pixel is defined as valid (part of the frame) when both LVAL and FVAL signals are at a high level.
3. The maximum latency (Td) of 1 readout line time defined below depends on the binning mode. In binning 1 x 1 mode, this delay is around 104 µs.
4. Minimum time at low level of LVAL signal is 10 µs (transfer time between two lines).
5. Minimum time at low level of FVAL signal is 4 lines readout time (around 416 µs).
6. Shutter delay is adjustable via serial communication commands (1, 5, 10 or 20 ms).

### Continuous: T=0

The camera delivers frames continuously:

- Frame N+1 integration starts as soon as the readout of frame N has been completed.
- The integration time is set by serial communication.
- The video lines (before and after the valid frame) are 4 + 4 for binning 1 x 1 (and also 1 + 1 for binning 4 x 4).

**Figure 12.** CameraLink Continuous Timing Diagram

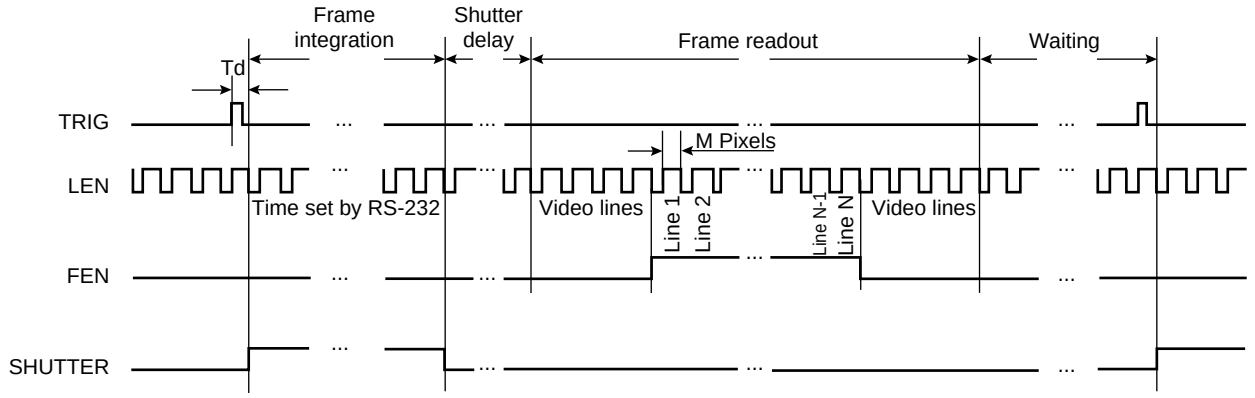


**Operation with External Trigger: T=1**

The start of integration is controlled by the user with the external signal TRIG:

- TRIG's rising edge activates the start of frame integration. This rising edge is synchronized by the camera with a latency of Td (time delay equivalent to a readout time for a line: see notes in Table 7 on page 19).
- The integration time is set by the serial communication.
- TRIG's signal period must be greater than the sum of the integration time and frame readout time.
- The video lines (before and after the valid frame) are 4 + 4 for binning 1 x 1 (and also 1 + 1 for binning 4 x 4).

**Figure 13.** CameraLink External Trigger Timing Diagram

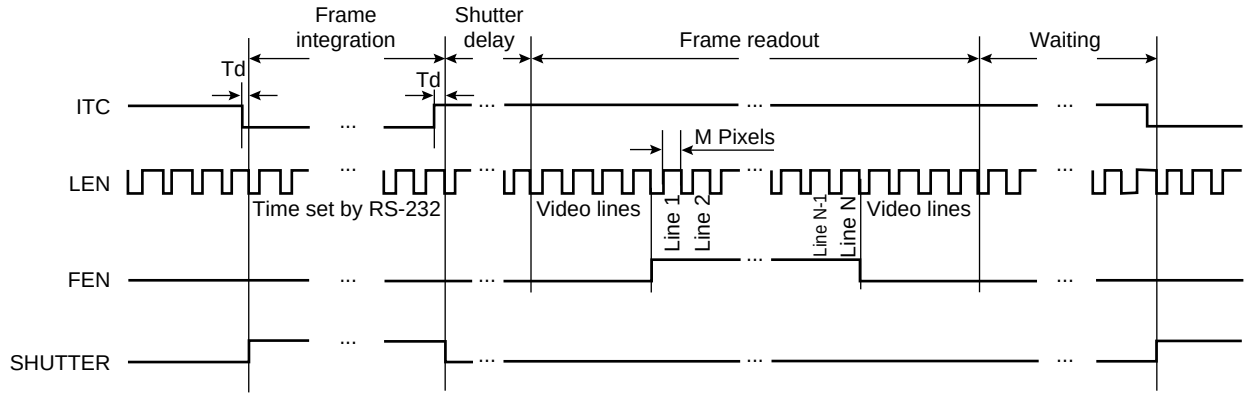



**Operation with Integration Time Control: T=2**

The integration is fully controlled by the user with the external signal ITC:

- ITC's falling edge activates the start of frame integration. This falling edge is synchronized by the camera with a latency of Td (time delay equivalent to a readout time for a line: see notes in Table 7 on page 19).
- ITC's rising edge activates the stop of the frame integration. This rising edge is synchronized by the camera with the same latency of Td.
- The ITC signal period must be greater than the sum of the integration time (defined by ITC low) and frame readout time.
- The video lines (before and after the valid frame) are 4 + 4 for binning 1 x 1 (and also 1 + 1 for binning 4 x 4).

**Figure 14.** CameraLink Integration Time Control Timing Diagram

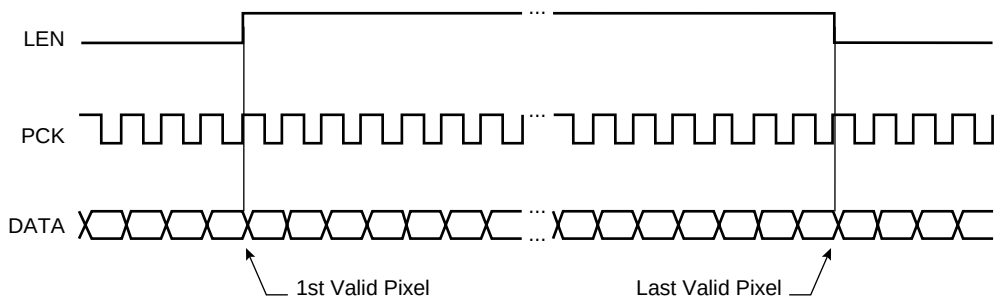


**Line Timing**

- The PCK's duty cycle is 50%
- The PCK's clock rate is 25 MHz
- The data rate (internal pixel clock) is 25 MHz in binning mode 1 x 1

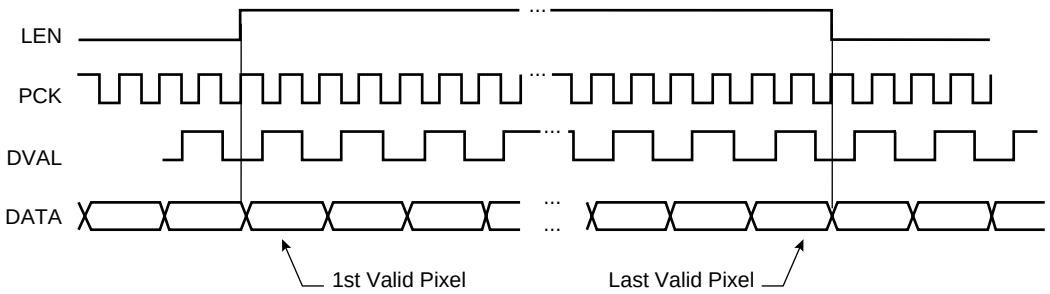
- Binning mode 1 x 1:
  - The data rate is 25 MHz
  - DVAL is always in high state

**Figure 15.** CameraLink Line Timing Diagram for Binning 1 x 1




- Binning mode 2 x 2 (and 4 x 4):
  - The data rate is 12.5 MHz (or 6.25 MHz)

**Figure 16.** CameraLink Line Timing Diagram for Binning 2 x 2 (and 4 x 4)



# Electrical Interfaces

## DATA, SYNC and TTL CONTROL for LVDS Cameras

**Table 8.** Specifications

| Symbol | I/O | Definition | Level |
|---|---|---|---|
| TRIG_ITC | I | Timing control:<br>- TRIG_ITC is either an external trigger or integration time control (ITC) depending on the timing mode configured via RS-232.<br>Operation with external trigger:<br>- TRIG_ITC = TRIG<br>Operation with ITC:<br>- TRIG_ITC = ITC<br>- TRIG_ITC is synchronized by the camera line clock (jitter: 104 µs) | LVDS(1) and TTL |
| PDATA(11..0) | O | Digital video output: 12-bit<br>8 bits output format: PDATA [ 7...0] | LVDS |
| FEN | O | Frame enable:<br>- FEN = 0: frame data valid: active lines<br>- FEN = 1: frame data not valid | LVDS |
| LEN | O | Line enable:<br>- LEN = 0: line data valid: active pixels<br>- LEN = 1: line data not valid | LVDS |
| PCK | O | Pixel clock | LVDS |
| SHUTTER | O | Shutter open/close:<br>- shutter open = 1<br>- shutter closed = 0<br>Delay between the falling edge of SHUTTER and the start of readout:<br>- 4 positions: 1, 10, 20 or 40 ms (set via RS-232) | LVDS and TTL |
| COLOUR_I(1..0) | I | Color selection of the next frame (in color mode):<br>- 00: red<br>- 01: green<br>- 10: blue<br>- 11: user defined | LVDS and TTL |
| COLOUR_O(1..0) | O | Color identification of the current frame (in color mode):<br>- 00: red<br>- 01: green<br>- 10: blue<br>- 11: user defined | LVDS and TTL |

Note: 1. LVDS (Low Voltage Differential Signal): EIA 644 standard.

All digital I/Os are differential: (signal+, signal-). Specifications are given for signal+.

LVDS drivers/receivers:

- Manufacturer: National Semiconductor / Driver: DS90LVO47ATMTC (SO16 package)

- Receiver: DS90LVO48ATMTC (SO16 package)

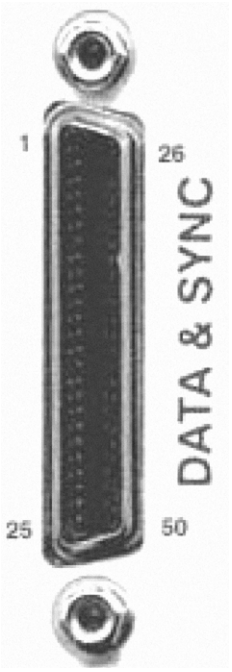
## DATA & SYNC Cabling

50-pin connector:

- Connector reference on camera: 3M 10250-6212JL (or 3M 10250-6212VC)
- Mating connector on cable side: 3M 10150-6000EL; shell: 3M 10350-A200-00

Atmel recommends using a twisted pair shielded cable.

**Table 9.** Pinout

| Pin Number | Signal | I/O | Pin Number | Signal | I/O | |
|---|---|---|---|---|---|---|
| 1 | PCK+ | O | 26 | LEN+ | O |  |
| 2 | PCK- | O | 27 | LEN- | O | |
| 3 | FEN+ | O | 28 | COLOUR_O1+ | O | |
| 4 | FEN- | O | 29 | COLOUR_O1- | O | |
| 5 | COLOUR_O2+ | O | 30 | GROUND | O | |
| 6 | COLOUR_O2- | O | 31 | GROUND | O | |
| 7 | PDATA0+ | O | 32 | PDATA1+ | O | |
| 8 | PDATA0- | O | 33 | PDATA1- | O | |
| 9 | PDATA2+ | O | 34 | PDATA3+ | O | |
| 10 | PDATA2- | O | 35 | PDATA3- | O | |
| 11 | PDATA4+ | O | 36 | PDATA5+ | O | |
| 12 | PDATA4- | O | 37 | PDATA5- | O | |
| 13 | PDATA6+ | O | 38 | PDATA7+ | O | |
| 14 | PDATA6- | O | 39 | PDATA7- | O | |
| 15 | PDATA8+ | O | 40 | PDATA9+ | O | |
| 16 | PDATA8- | O | 41 | PDATA9- | O | |
| 17 | PDATA10+ | O | 42 | PDATA11+ | O | |
| 18 | PDATA10- | O | 43 | PDATA11- | O | |
| 19 | GROUND | – | 44 | NC | – | |
| 20 | GROUND | – | 45 | NC | – | |
| 21 | SHUTTER+ | O | 46 | TRIG_ITC+ | I | |
| 22 | SHUTTER- | O | 47 | TRIG_ITC- | I | |
| 23 | COLOUR_I1+ | I | 48 | COLOUR_I2+ | I | |
| 24 | COLOUR_I1- | I | 49 | COLOUR_I2- | I | |
| 25 | NC | – | 50 | NC | – | |

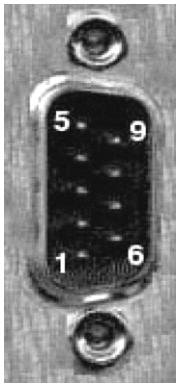


Note: NC: not connected

## TTL CONTROL Cabling

The connector on the camera is a D-sub 9-pin male connector.

**Table 10.** Pinout

| Pin Number At Camera Output | Signal | Direction | |
|---|---|---|---|
| 1 | SHUTTER | Out |  |
| 2 | TRIG-ITC | In | |
| 3 | COLOUR-I1 | In | |
| 4 | COLOUR-I2 | In | |
| 5 | NC | – | |
| 6 | NC | – | |
| 7 | COLOUR-O1 | Out | |
| 8 | COLOUR-O2 | Out | |
| 9 | GROUND | – | |



Notes:
1. The following signals: TRIG-ITC, COLOUR-I1, COLOUR-I2 are provided by the DATA & SYNC (MDR50) connector in LVDS format or by the TTL CONTROL connector; the two different signals are logically “anded” as follows: TRIG-ITC from LVDS and TRIG-ITC from TTL. The inputs left open are internally tied to a high level.
2. The SHUTTER, COLOUR-O1 and COLOUR-O2 outputs are available on both DATA & SYNC and TTL output connectors.

**Warning**

- I/O signals are 3.3V TTL compatible with 5V TTL standard
- ±24 mA output driver
- Maximum voltage range: -0.5V to 7V. Safety of the camera is not guaranteed beyond these values.
- Supports live insertion
- Ground connected to power supply GROUND and RS232 GROUND.

## CAMERALINK and TTL CONTROL for CameraLink Camera

**Table 11.** Specifications

| Symbol | I/O | Definition | Level |
|---|---|---|---|
| TRIG_ITC(1) | I | Timing control:<br>- TRIG_ITC is either an external trigger or integration time control (ITC) depending on the timing mode configured via serial communication.<br>Operation with external trigger:<br>- TRIG_ITC = TRIG<br>Operation with ITC:<br>- TRIG_ITC = ITC<br>- TRIG_ITC is synchronized by the camera line clock (jitter: 104 µs) | LVDS(5) and TTL |
| PDATA(11..0) | O | Digital video output: 12-bit<br>8 bits output format: PDATA [7...0] | LVDS |
| FVAL | O | Frame enable:<br>- FVAL = 1: frame data valid: active lines<br>- FVAL = 0: frame data not valid | LVDS |
| LVAL | O | Line enable:<br>- LVAL = 1: line data valid: active pixels<br>- LVAL = 0: line data not valid | LVDS |
| DVAL | O | Data strobe:<br>- DVAL = 1: pixel data valid<br>- DVAL = 0: pixel data not valid | LVDS |
| PCK | O | Pixel clock | LVDS |
| SHUTTER | O | Shutter open/close:<br>- shutter open = 1<br>- shutter closed = 0<br>Delay between the falling edge of SHUTTER and the start of readout:<br>- 4 positions: 1, 10, 20 or 40 ms (set via serial communication) | TTL |
| COLOUR_I(1..0)(2)(3) | I | Color selection of the next frame (in 3-shot color mode):<br>- 00: red<br>- 01: green<br>- 10: blue<br>- 11: user defined | LVDS and TTL |
| COLOUR_O(1..0)(4) | O | Color identification of the current frame (in 3-shot color mode):<br>- 00: red<br>- 01: green<br>- 10: blue<br>- 11: user defined | LVDS and TTL |

Notes:
1. TRIG_ITC signal is connected on CC1 differential inputs
2. COLOUR_I0 signal is connected on CC2 differential inputs
3. COLOUR_I1 signal is connected on CC3 differential inputs
4. COLOUR_O0 and COLOUR_O1 signals are coded as outputs PDATA(13,12)

5. LVDS (Low Voltage Differential Signal): EIA 644 standard

All digital I/Os are differential: (signal+, signal-). Specifications are given for signal+.

CameraLink drivers/receivers:

- Driver: National Semiconductor DS90CR285MTD (SO56 package)
- Receiver: National Semiconductor DS90LVO48ATMTC (SO16 package)

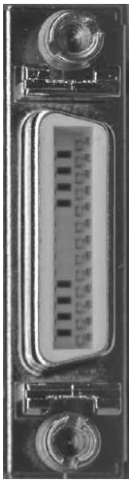
## CameraLink Cabling

26-pin connector:

- Connector reference on camera: 3M 10226-2210VE

Atmel recommends using a CameraLink standard shielded cable such as the 3M 14X26-SZLB-XXX-0LC.

**Table 12.** Pinout

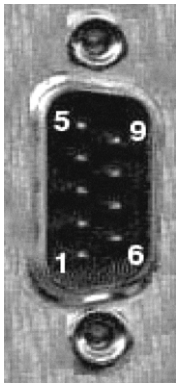
| Pin Number | Signal | I/O | Pin Number | Signal | I/O | |
|---|---|---|---|---|---|---|
| 1 | GROUND | – | 14 | GROUND | – |  |
| 2 | X0- | O | 15 | X0+ | O | |
| 3 | X1- | O | 16 | X1+ | O | |
| 4 | X2- | O | 17 | X2+ | O | |
| 5 | XCLK- | O | 18 | XCLK+ | O | |
| 6 | X3- | O | 19 | X3+ | O | |
| 7 | SERTC+ | I | 20 | SERTC- | I | |
| 8 | SERTFG- | O | 21 | SERTFG+ | O | |
| 9 | CC1- | I | 22 | CC1+ | I | |
| 10 | CC2+ | I | 23 | CC2- | I | |
| 11 | CC3- | I | 24 | CC3+ | I | |
| 12 | CC4+ | I | 25 | CC4- | I | |
| 13 | GROUND | – | 26 | GROUND | – | |

Note: NC: not connected

## TTL CONTROL Cabling

The connector on the camera is a D-sub 9-pin male connector.

**Table 13.** Pinout

| Pin Number At Camera Output | Signal | Direction | |
|---|---|---|---|
| 1 | SHUTTER | Out |  |
| 2 | TRIG-ITC | In | |
| 3 | COLOUR-I1 | In | |
| 4 | COLOUR-I2 | In | |
| 5 | NC | – | |
| 6 | NC | – | |
| 7 | COLOUR-O1 | Out | |
| 8 | COLOUR-O2 | Out | |
| 9 | GROUND | – | |



Notes:
1. The following signals: TRIG-ITC, COLOUR-I1, COLOUR-I2 are provided by the DATA & SYNC (MDR26) connector in LVDS format or by the TTL CONTROL connector; the two different signals are logically “anded” as follows: TRIG-ITC from LVDS and TRIG-ITC from TTL. The inputs left open are internally tied to a high level.
2. COLOUR-O1 and COLOUR-O2 Outputs are available on both CameraLink and TTL Output Connectors.

### Warning

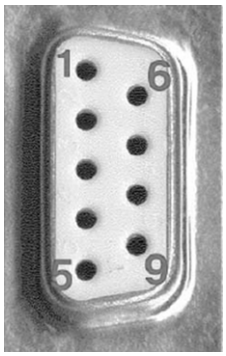
- I/O signals are 3.3V TTL compatible with 5V TTL standard
- ±24 mA output driver
- Maximum voltage range: -0.5V to 7V. Safety of the camera is not guaranteed beyond these values.
- Supports live insertion
- Ground connected to power supply GROUND.

## RS-232 for LVDS Camera

- On camera side: D-sub 9 pins female
- On compute side: D-sub 9 pins male, pinout compatible with the computer's serial port

Note: The cable to be used is a straight pin-to-pin male-female cable.

**Table 14.** Pinout

| Pin Number<br>At camera output | Signal | |
|---|---|---|
| 1 | NC |  |
| 2 | TX | |
| 3 | RX | |
| 4 | NC | |
| 5 | GROUND | |
| 6 | NC | |
| 7 | NC | |
| 8 | NC | |
| 9 | NC | |

Notes: 1. NC: not connected
2. Pins 7 and 8 are internally shorted.

## Power Supply

### Specifications

**Table 15.** Power Supply Specifications

| Parameter | Nominal Value | Min Value | Max Value |
|---|---|---|---|
| Voltage | +24V | +20V | +28V |
| Current | 0.23A | 0.26A | 0.20A |

### Cabling

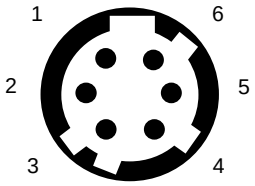
- Camera connector type: Hirose HR10A-7R-6PB (male)
- Cable connector type: Hirose HR10A-7P-6S (female)

**Table 16.** Pinout

| Pin Number | Signal | Pin Number | Signal |
|---|---|---|---|
| 1 | PWR | 4 | GND |
| 2 | NC | 5 | NC |
| 3 | PWR | 6 | GND |

Note: NC: not connected

**Figure 17.** Receptacle Viewed from Behind the Camera




**Caution**: power supply cabling is fully compatible with Atmel's AviivA Linescan Cameras. The cabling is NOT compatible with the preceding Camelia 8M.

An internal 1-amp fuse protects the camera against high currents.

An internal diode protects the camera against cabling inversions.

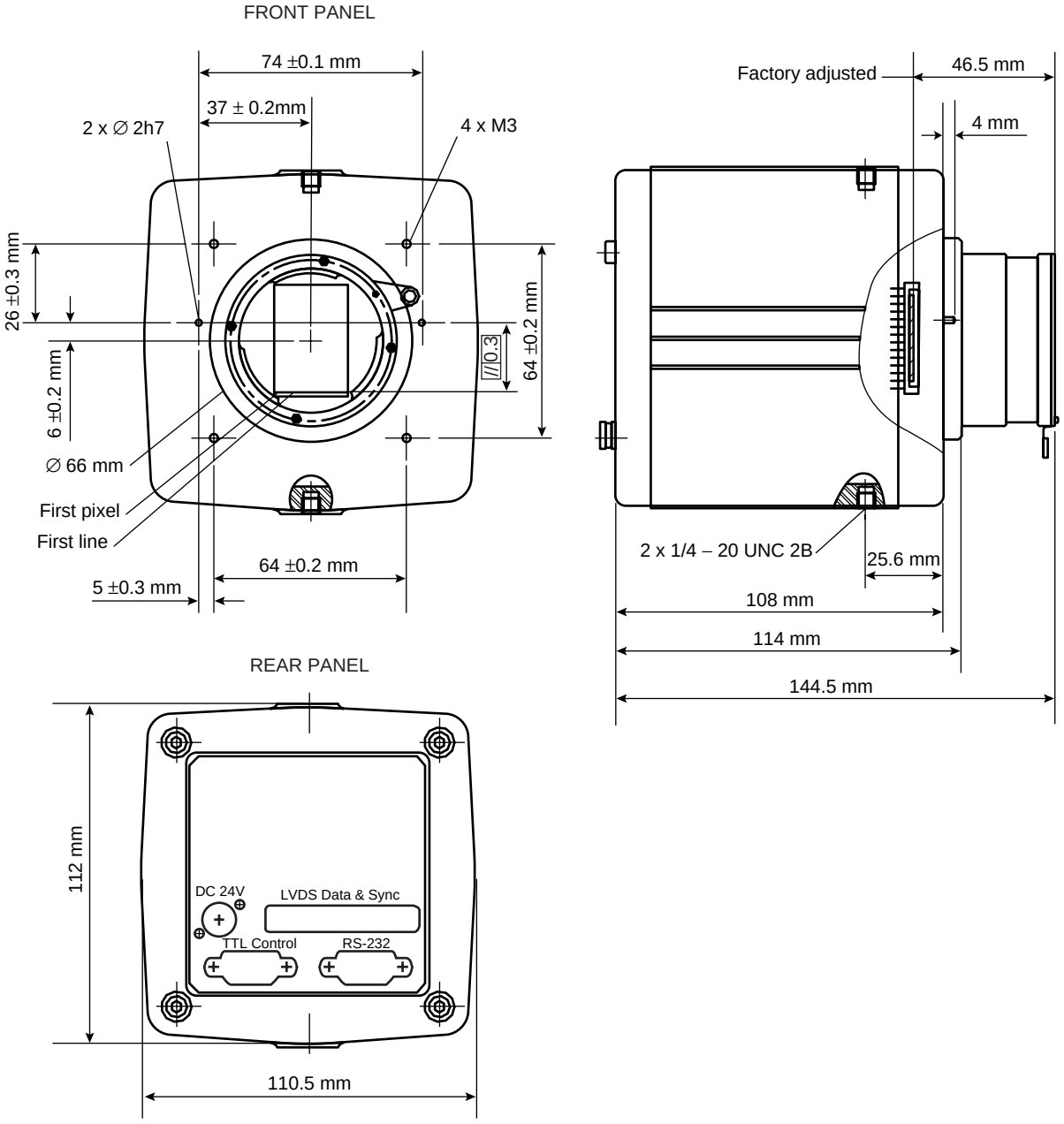
## Cable Kits

- LVDS-FGT: FGT frame grabber Black and White + DATA & SYNC for FGT frame grabber (length 2.5 meters) + power supply (length 10 meters, open on power supply side)
- CameraLink: CameraLink (length 5 meters) + power supply (length 10 meters, open on power supply side)
- Connectors LVDS: 3M MDR 50 + HR10A-7P-6S

# Mechanical Interface

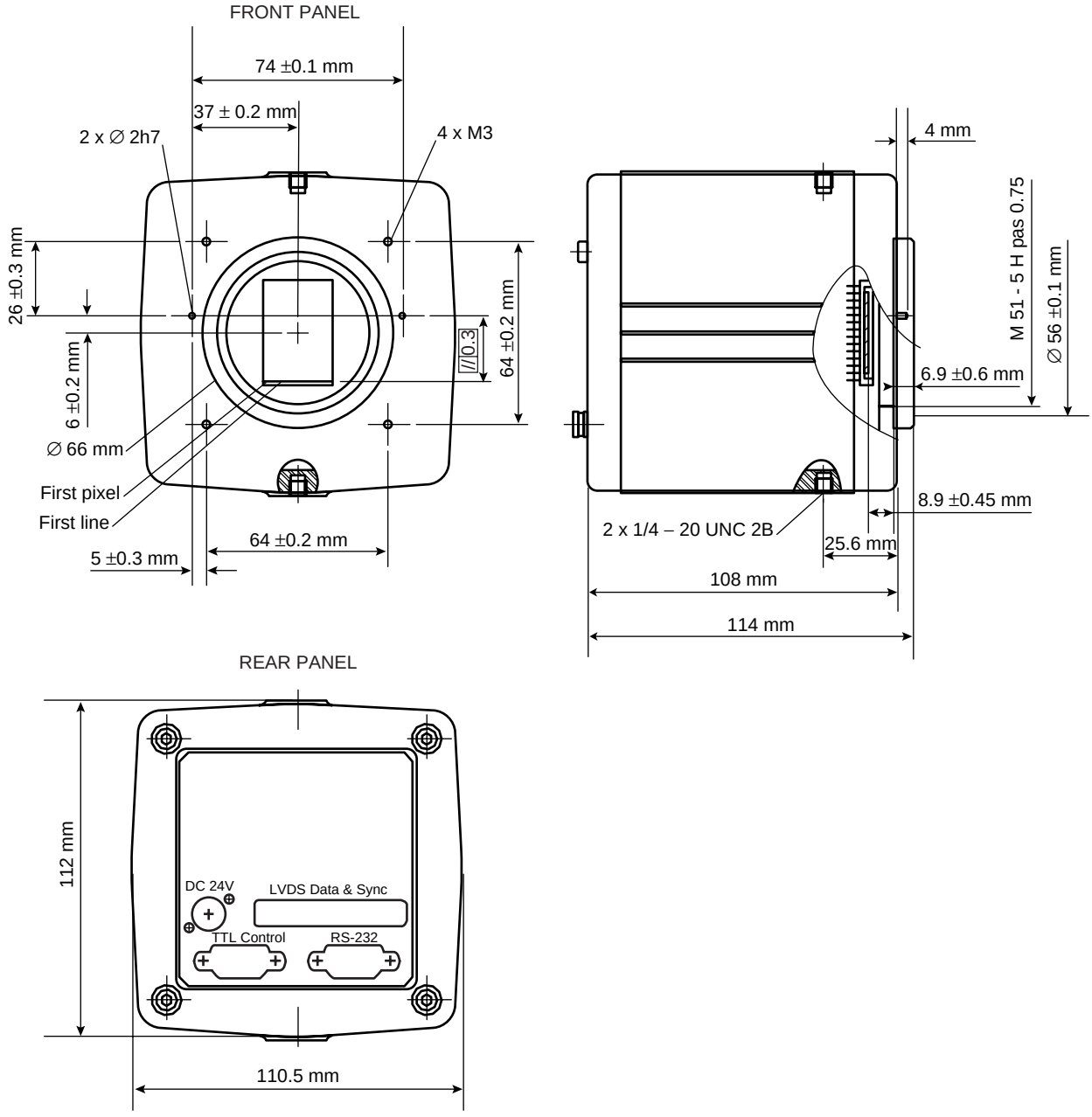
## LVDS Camera with F Mount Ring

**Figure 18.** With F Mount Ring



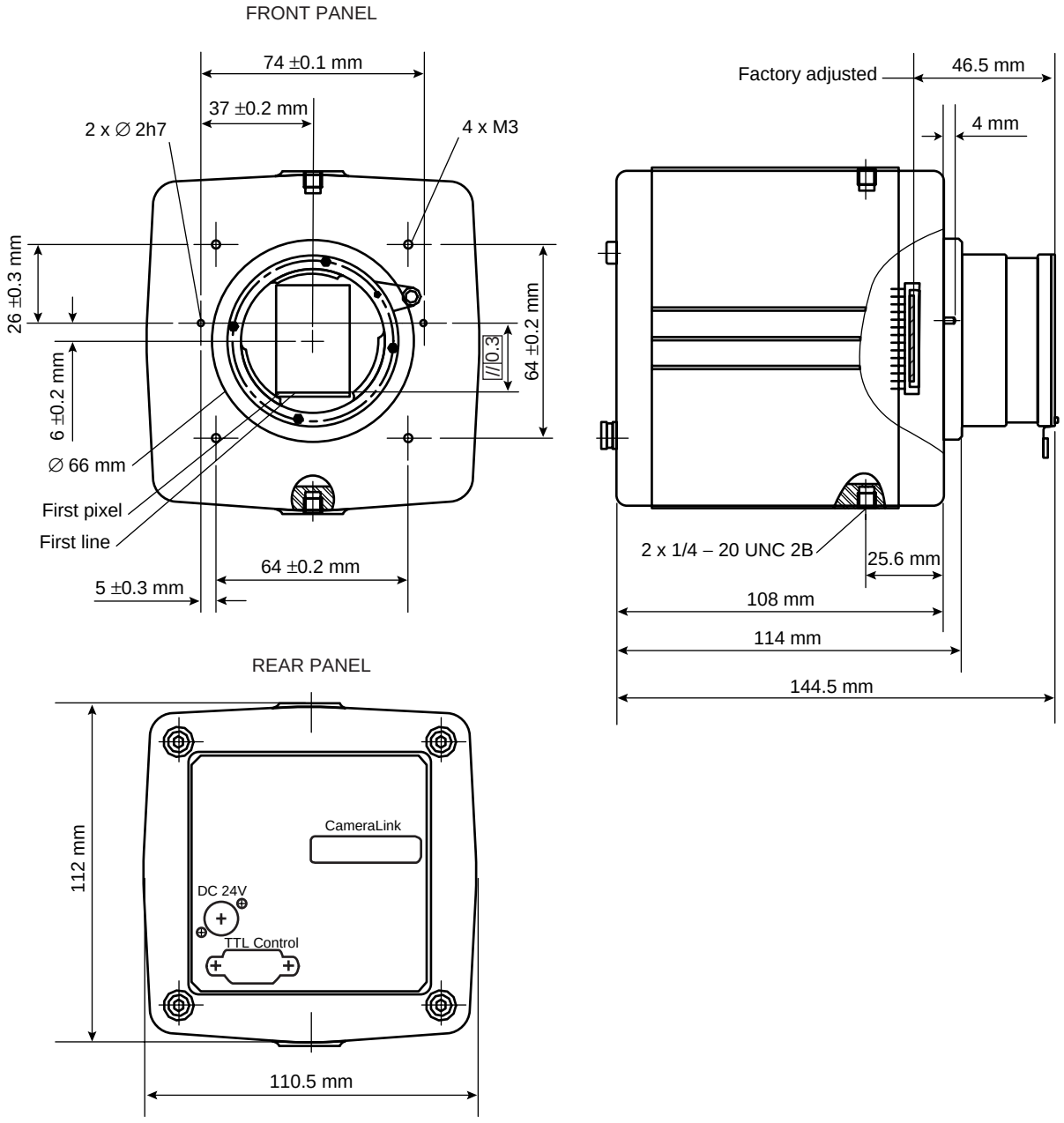
## LVDS Camera without F Mount Ring

**Figure 19.** Without F Mount Ring



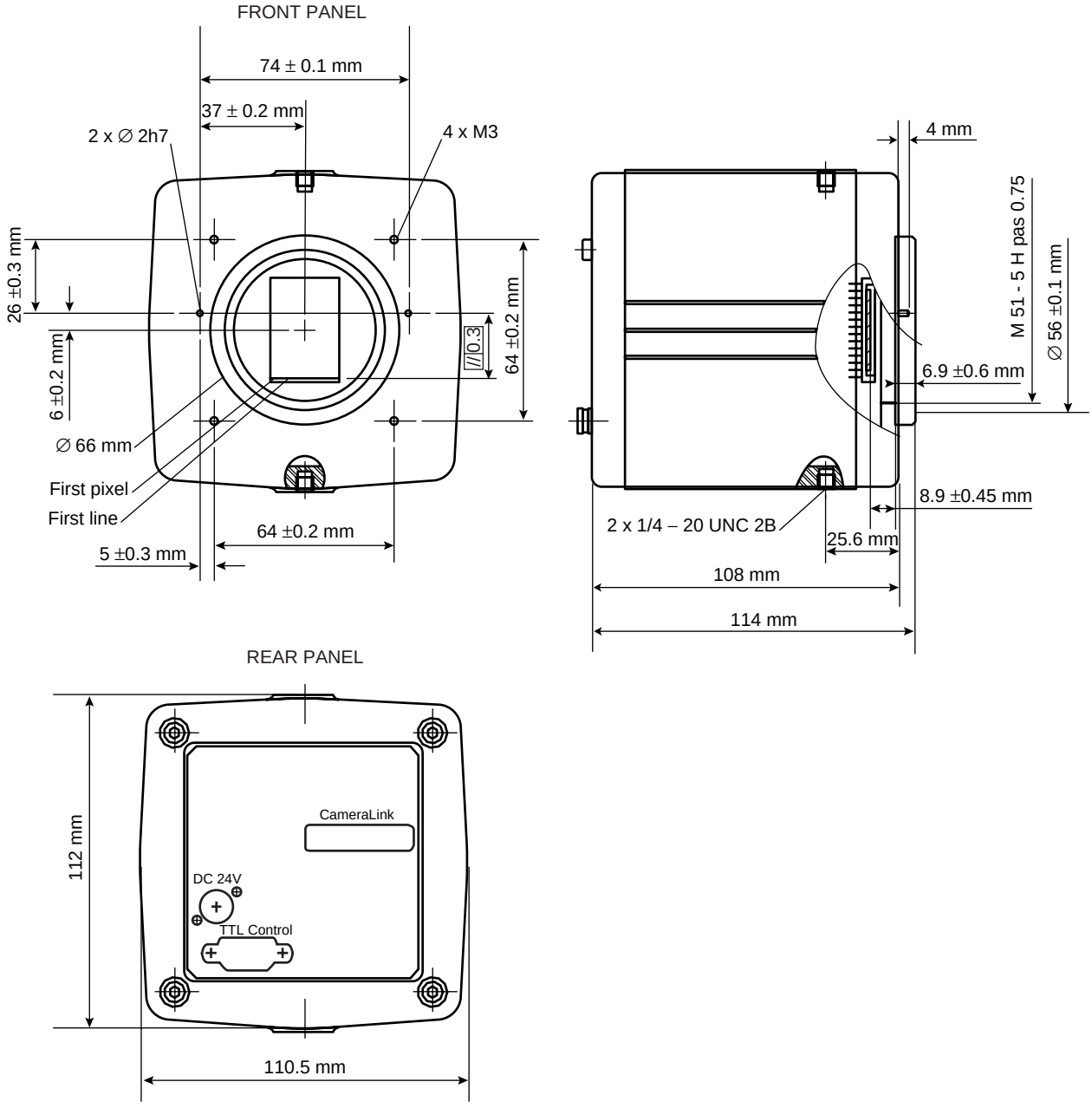
## CameraLink Camera with F Mount Ring

**Figure 20.** With F Mount Ring



## CameraLink Camera without F Mount Ring

**Figure 21.** Without F Mount Ring



## Mechanical Mounting References

- Position in the X and Y plan:
  - The center pixel of the CCD sensor is positioned within a circle centered on the optical axis and with a diameter of 0.35 mm. The optical axis is defined by the mechanical thread for the optical adapter.
  - The center pixel of the CCD sensor is referenced to the two needles on the front panel with a tolerance of ±0.125 mm.
- Position in the Z plan:
  - For cameras delivered with an F mount ring, the distance from the CCD sensor plan to the Nikon mount is set in factory at 46.5 mm.
  - For cameras delivered without the F mount ring, the distance from the CCD sensor plan to the front plan of the thread is 8.9 ±0.45 mm.
- Tilt around the Z axis:
  - All of the CCD sensor's pixels are located between two plans, perpendicular to the optical axis and separated by a maximum distance of 0.26 mm.

## Standard Conformity

The cameras have been tested with the following equipment:

- Complete Atmel casing
- Shielded power supply cable
- Shielded and twisted pair data transfer cable
- TTL CONTROL cable
- Linear AC-DC power supply

We recommend using the above configuration to ensure compliance with the standards hereafter.

### CE conformity

The Camelia camera complies with the European directive 89/336/CEE (EN55022 B/CISPR22 B, EN55024).

Class A of EN55022 is obtained without condition. Class B of EN55022 is obtained with ferrite beads on the DATA/SYNC and TTL CONTROL cables.

### FCC conformity

The Camelia camera complies with Part 15 of the FCC rules, which states that:

“Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

**Warning**: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.”

## Ordering Information

**Table 17.** Ordering Codes

| Part Number | Description |
|---|---|
| AT71XM1LV8MFERCB0 | CAMELIA 8M M1 LVDS Grade E with Housing and F-Mount |
| AT71XM1LV8MFERCA0 | CAMELIA 8M M1 LVDS Grade E with Housing and no F-Mount |
| AT71XM1LV8MFERAA0 | CAMELIA 8M M1 LVDS Grade E without Mechanics |
| AT71XM1CL8MFERCB0 | CAMELIA 8M M1 CameraLink Grade E with Housing and F-Mount |
| AT71XM1CL8MFERCA0 | CAMELIA 8M M1 CameraLink Grade E with Housing and no F-Mount |
| AT71XM1CL8MFERAA0 | CAMELIA 8M M1 CameraLink Grade E without Mechanics |
| AT71-LV-P2C1D1B2 | LVDS-FGT Kit (see “Cable Kits” on page 29) |
| AT71-LV-P8C8D8A0 | Set of LVDS connectors (see “Cable Kits” on page 29) |
| AT71-CL-P2C0D3A0 | CL Kit (see “Cable Kits” on page 29) |

## Revision History

| Version Number | Description |
|---|---|
| 5319C | M = 3 command for 8-bit output format |
| 5319C | Gain range = -6.1 dB to 27 dB |

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